IN THE CLAIMS

1. (Currently amended) A back annotation apparatus including:

a pre-layout simulation implementing part for carrying out a pre-layout simulation to detect ~~detecting~~ nodes of which the potential changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation;

a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of said logical circuit;

a parasitic element extraction part connected to said pre-layout simulation implementing part which extracts parasitic elements from said nodes detected during the pre-layout simulation ~~of which the potential changes~~;

a net list generation part connected to said parasitic element extraction part for generating a net list which includes all the devices included in layout pattern data and parasitic elements extracted in said parasitic element extraction part; and

a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list.

2. (Original) A back annotation apparatus according to Claim 1, wherein

said pre-layout simulation implementing part includes:

an active node detection part for detecting nodes of which the potential changes when a predetermined signal is applied to said logic circuit; and

a non active node detection part for detecting nodes of which the potential does not change when said predetermined signal is applied to said logic circuit,

said net list generation part includes a net list generation part with parasitic elements which is connected to said parasitic element extraction part and said layout pattern verification implementing part and which generates a net list including parasitic elements to the active nodes within said layout pattern data and devices connected to said active nodes,

said post layout simulation implementing part includes a circuit which is connected to said net list generation part and said non active node detection part, which fixes the potential of said node, of which the potential does not change, at a predetermined potential and which implements a post layout simulation by using said net list.

3. (Original) A back annotation apparatus according to Claim 2 further including:

an internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to said layout pattern verification implementing part and to which serially connected devices degenerated according to a predetermined standard at the time of layout pattern verification are connected in parallel; and

a node information updating part for updating the detection result of the active node detection part and the non active node detection part based on the extraction result at said internal node extraction part, which is connected to said internal node extraction part, said active node detection part and said non active node detection part.

4. (Original) A back annotation apparatus according to Claim 2 further including:

an internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to said layout pattern verification implementing part and wherein serially connected elements degenerated according to a predetermined standard at the time of layout pattern verification are made to be a single element; and

a node information updating part for updating the detection result of the active node detection part and the non active node detection part based on the extraction result at said internal node extraction part, which is connected to said internal node extraction part, said active node detection part and said non active node detection part.

5. (Original) A back annotation apparatus according to Claim 2 further including:

a first internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to said layout pattern verification implementing part and to which serially connected devices degenerated according to a predetermined standard at the time of layout pattern verification are connected in parallel;

a second internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to said layout pattern verification implementing part and wherein serially connected elements degenerated according to a predetermined standard at the time of layout pattern verification are made to be a single element;

a node information updating part for updating the detection result of the active node detection part and the non active node detection part based on the extraction result at said first

and said second internal node extraction parts, which is connected to said first internal node extraction part, said second internal node extraction part, said active node detection part and said non active node detection part; and

a parasitic element information degenerating part for degenerating only the parasitic element information included in said net list which is connected to said net list generation part with parasitic elements.

6. (Currently amended) A back annotation method including:

the step of performing a pre-layout simulation to detect ~~detection of~~ nodes of which the potential changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation;

the step of implementing a predetermined layout pattern verification with respect to a layout pattern of said logic circuit;

the step of extracting parasitic elements from said nodes detected during the pre-layout simulation ~~of which the potential changes~~;

the step of generation of a net list including all the devices included in layout pattern data and the parasitic elements extracted in said step of extracting parasitic elements; and

the step of implementation of a post layout simulation by using said net list.

7. (Original) A back annotation method according to Claim 6, wherein:

said step of detection includes;

the step of detection of nodes of which the potential changes when said predetermined signal is applied to said logic circuit; and

the step of detection of nodes of which the potential does not change when said predetermined signal is applied to said logic circuit,

said step of generation includes the step of generation of a net list which includes parasitic elements on the active nodes within said layout pattern data and devices connected to said active nodes, and

said step of implementation includes the step of fixing the potential of said nodes, of which the potential does not change, at a predetermined potential and implementing a post layout simulation by using said net list.

8. (Previously presented) A back annotation method according to Claim 7 further including:

the step of extraction of layout pattern data or nodes of a logic circuit diagram, wherein serially connected devices, which are degenerated according to a predetermined standard at the time of layout pattern verification, are connected in parallel; and

the step of updating information with respect to said nodes of which the potential changes and said nodes of which the potential does not change based on the result of extraction of the nodes.

9. (Previously presented) A back annotation method according to Claim 7 further including:

the step of extraction of layout pattern data or nodes of a logic circuit diagram, wherein serially connected elements, which are degenerated according to a predetermined standard at the time of layout pattern verification, are made to be a single element; and

the step of updating information with respect to said nodes of which the potential changes and said nodes of which the potential does not change based on the result of extraction of the nodes.

10. (Previously presented) A back annotation method according to Claim 7 further including:

the step of extraction of layout pattern data or nodes of a logic circuit diagram, wherein serially connected devices, which are degenerated according to a predetermined standard at the time of layout pattern verification, are connected in parallel;

the step of extraction of layout pattern data or nodes of a logic circuit diagram, wherein serially connected elements, which are degenerated according to a predetermined standard at the time of layout pattern verification, are made to be a single element;

the step of updating information with respect to said nodes of which the potential changes and said nodes of which the potential does not change based on the result of extraction of the nodes; and

the step of degeneration of only parasitic element information included in said net list.